What is claimed is:

1. A schematic for an integrated circuit, comprising:

a plurality of circuit components interconnected by lines;

a plurality of width markers, each line assigned a width marker; and

each width marker having a minimum width parameter.

2. The schematic of claim 1, wherein at least one of the lines has a width requirement greater than a default minimum line width.

3. The schematic of claim 1, wherein at least one of the lines has an associated width of a default minimum width.

4. A schematic for an integrated circuit, comprising:

a plurality of circuit components interconnected by lines; and

a line width layer, comprising:

a plurality of line width markers, a line width marker for each line having a width greater than a default minimum width; and

a line width parameter for each line width marker.

5. The schematic of claim 4, wherein at least one of the lines has a width requirement greater than a default minimum line width.

6. The schematic of claim 4, wherein at least one of the lines has an associated width of a default minimum width.

7. The schematic of claim 4, wherein each line width parameter represents a minimum line width for the line associated with that line width parameter.

8. The schematic of claim 4, wherein the line width layer is separate from the circuit components.

9. An integrated circuit layout, comprising:

a component layer comprising a plurality of circuit components interconnected by lines, each of the lines having an associated width; and

a line width layer separate from the component layer that stores the associated widths.

10. The integrated circuit layout of claim 9, wherein the associated width of at least one line is a minimum width that is greater than an absolute minimum line width.

11. An integrated circuit layout, comprising:

a component layer comprising a plurality of circuit components interconnected by lines; and

a line width layer comprising:

a plurality of line width markers, a line width marker for each line having a width greater than an absolute minimum width; and

a line width parameter for each line width marker.

12. The integrated circuit layout of claim 11, wherein each line width parameter represents a minimum line width for the line associated with that line width parameter.

13. The integrated circuit layout of claim 11, wherein the line width layer is separate from the component layer.

14. A schematic for an integrated circuit, comprising:

a plurality of symbols respectively corresponding to circuit components of the integrated circuit, the symbols interconnected by schematic lines respectively corresponding to circuit lines interconnecting the circuit components;

a plurality of width markers, each schematic line assigned a width marker; and

each width marker having a width parameter representing a minimum width for the circuit line corresponding to the schematic line for that width marker.

15. The schematic of claim 14, wherein the minimum width represented by each width parameter is greater than a default minimum width.

16. A schematic for an integrated circuit, comprising:

a plurality of symbols respectively corresponding to circuit components of the integrated circuit, the symbols interconnected by schematic lines respectively corresponding to circuit lines interconnecting the circuit components; and

a line width layer, comprising:

a plurality of line width markers, a line width marker for each schematic line corresponding a circuit line having a width greater than a default minimum width; and

a line width parameter for each line width marker.

17. The schematic of claim 16, wherein each line width parameter represents a minimum line width for the circuit line corresponding to the schematic line associated with that line width parameter.

18. The schematic of claim 16, wherein the line width layer is separate from the symbols.